REMARKS

Receipt of the office action mailed December 2, 2003, is acknowledged. Claims 1-5 are pending in the application. Claims 1-4 have been objected to. Claims 1-2 and 4-5 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Sakurai, U.S. Patent 5,999,472 ("Sakurai"). New claims 6 and 7 have been added. In keeping with the foregoing amendments and the following remarks, claims 1, 2 and 4-7 are in condition for allowance.

Claim 3 has been cancelled. Claims 6 and 7 have been added.

Claim 1 has been objected to for reciting "N buffer means" without any antecedent basis. Claim 1 has been amended to now consistently recite "a plurality of buffer means" at the first instance of reciting this element and "the plurality of buffer means" in the remaining recitations of this element in the claim. The noted amendment to claim 1 overcomes the objection made thereto in the Office action. Therefore, the objection to claim 1 should be withdrawn.

Claims 2-4 have been objected to for failing to provide a definition for possible values of "N" as recited. Claim 2 has been amended to recite that N is a positive integer and the counter is (N-1)-nary, if the number of the plurality of banks is 2^N. Accordingly, with claims 2 as amended, a "zero-nary" counter is not possible. Accordingly, the amendment to claim 2 overcomes the objection made thereto in the Office action. Therefore, the objection to claim 2 and claim 4, which depends from claim 2, should not be withdrawn.

Claims 1, 2, 4 and 5 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Sakurai. Claim 1 has been amended to recite that each input buffer means includes a latch means for sustaining the output signals of the plurality of input

buffer means within a certain period of time only when the refresh command signals are applied. In contrast, Sakurai does not disclose or even suggest that each input buffer means includes a latch means as recited in claim 1.

Referring to FIGS. 15 of Sakurai (also shown in FIG. 3), a multiplexer 10 receives a refresh row address signal RADi from a refresh counter 9 and a row address signal ADi from an address buffer 6 (shown as 106 in FIG. 5) and supplies a row address signal to a latch circuit 103 in response to a latch instruction signal RAL. Thus, the latch circuit 103 of Sakurai is not included with the address buffer 6 (shown as 106 in FIG. 5) to sustain the output signals of the address buffer. In contrast, claim 1 recites that each input buffer means includes a latch means for sustaining the output signals of the plurality of input buffer means within a certain period of time only when the refresh command signals are applied.

Because Sakurai does not disclose that each input buffer means includes a latch means for sustaining the output signals of the plurality of input buffer means within a certain period of time only when the refresh command signals are applied, Sakurai does not disclose every element of claim 1. Therefore, claim 1 is patentable over Sakurai and rejection of claim 1, and claims 2, 4 and 6 depending therefrom should be withdrawn.

Claim 5 recites, in part, buffering N bank address signals inputted from the external circuit with the refresh command signals. In contrast, Sakurai does not disclose or even recite the above-noted step of claim 5.

As described above and with reference to FIGS. 3 and 15 of Sakurai, an address buffer 6 (shown as 106 in FIG. 5) performs the buffering of address signals AD. A multiplexer 10 receives a refresh row address signal RADi from a refresh counter 9 and

a row address signal ADi from an address buffer 6 (shown as 106 in FIG. 5) and supplies a row address signal to a latch circuit 103 in response to a latch instruction signal RAL. Accordingly, Sakurai does not buffer each row address signal with a refresh command signal. In contrast, claim 5 recites buffering N bank address signals inputted from the external circuit with the refresh command signals. Because Sakurai does not disclose buffering N bank address signals inputted from the external circuit with the refresh command signals, Sakurai does not disclose every element of claim 5. Therefore, claim 5 is patentable over Sakurai and rejection of claim 5, and claim 7 depending therefrom should be withdrawn.

In view of the foregoing, claims 1, 2 and 4-7 as presented herein are in good and proper form for allowance. A favorable action on the part of the Examiner is respectfully solicited.

The Examiner is invited to contact the undersigned at the telephone number listed below in order to discuss any remaining issues or matters of form that will place this case in condition for allowance.

Respectfully submitted,

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